

A Review of Current Mode Circuits

Dr. T. S. Rathore, SMIEEE, FIETE

Independent Researcher, G-803, Country Park, Borivali E, Mumbai 400066 India

tsrathore@ee.iitb.ac.in

Abstract -- Advantages of Current Mode (CM) circuits are mentioned. Various methods of obtaining CM circuits from known voltage Mode (VM) circuits are reviewed. Unlike other methods, Rathore and Khot method does not involve nullator-norator pairs and require no additional elements. It maintains the same topology, and can handle various types of active devices. Theoretically, the performances of both VM and CM circuits are identical, however a better high-frequency performance is obtained from CM circuits when physical models of the active devices are considered.

Keywords: Voltage mode, Current mode, VM-CM pair

I. INTRODUCTION

WE shall be using the following definitions. A *voltage mode (VM)*, *current mode (CM) device* is that which gives voltage (current) as the output. The input(s) may be voltage(s) or current(s). These devices are shown in Fig. 1.

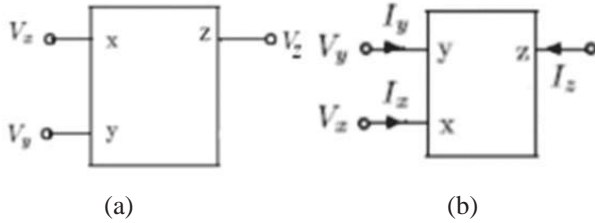


Figure 1. (a) VM device if $V_z = V_x$, $V_z = V_y$, or $V_z = (V_x \pm V_y)$
 (b) CM device if $I_z = I_x$, or $I_z = I_y$, or $I_z = (I_x \pm I_y)$

VM (CM) *circuit* is that which has both the input and output signals voltages (currents). Figure 2 shows simple VM and CM passive low pass filters. Lossless non-inverting integrators based upon the trans-conductance amplifier and a capacitor in VM and CM are shown in Fig. 3. More complex circuits may use many VM and/or CM devices within them.

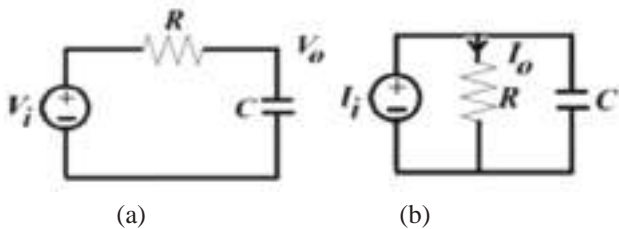


Figure 2. (a) VM low-pass filter (b) CM low-pass filter.

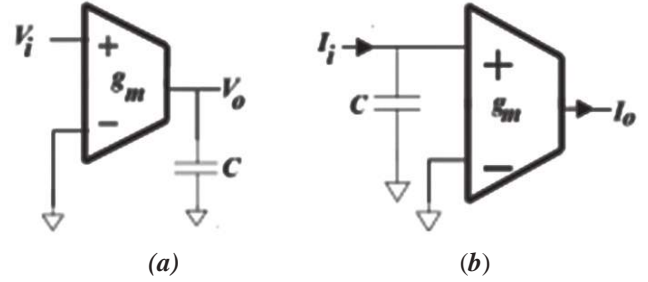


Figure 3. Non-inverting lossless (a) VM integrator (b) CM integrator.

II. ADVANTAGES

Advantages of CM structures: (i) In the VM circuits, the floating voltages can be summed by connecting them in series. However, when voltages have a common terminal, they require additional circuitry. In the CM circuits, summing of current signals requires only a node. (ii) The current signals can be easily replicated and scaled using current mirrors. Thus the CM structures are simpler than the VM ones. (iii) The CM devices have higher bandwidth and slew rate than VM devices. They can operate with low voltages. Hence the circuits employing CM devices are suitable for IC technology.

Advantages of processing the current signals: CM circuits are suitable for operation at higher frequencies and lower supply voltages. This can be explained as follows. Since node voltages are of no concern in current signal processing, circuits can be designed in which currents change with a signal, but the node voltages remain relatively very small. With small node voltages, the parasitic capacitances on the nodes require extremely small time to charge and discharge as the signal is processed. Hence the signal processing operations are not limited in speed in the same way if voltage signals were being processed. The low supply voltage operation is achieved because small voltages appear on the nodes. Therefore, the filters that process current signals have been developed.

Most authors that refer to CM filters have used current variables (specifically branch currents) when describing the operation of the circuits and invariably include only current equations when describing how a circuit operates. Often no mention of a voltage is made anywhere in the discussion of the operation of the circuit. Schumann and Tan [2] presented a brief overview

of a few important synthesis and implementation methods for current-based analog filters using trans-conductances. They did not state exclusively CM filters. A trans-conductance is a VM device, the filters are constructed such that each trans-conductance sees a load impedance that converts the output current into a voltage, which in turn becomes the input for the next trans-conductance stage. Thus, the signals alternate between voltages and currents.

In the beginning, essentially all filters were VM filters. In those applications where an input (output) port variable of interest was a current (voltage), a trans-resistance (trans-conductance) block was invariably added to the input (output) port to perform a current to voltage (voltage to current) conversion of the input (output) variable. Invariably, an analysis of these filters resulted in a set of linear equations in which the variables in the equations were node voltages. This was somewhat natural as most filter circuits have fewer nodes than branches, thus favouring a node analysis in which the variables are inherently the node voltages.

It may be noted from two low pass filters of Fig. 2 that the pole location is identical irrespective of whether the individual components operate in a CM or VM. Thus, at least in this example, the performance is not affected by the mode of operation. The poles of the filter do not have units of current or voltage and are the same whether obtained from an analysis involving current variables or from voltage variables or from a mixture of the two. Unlike the simple circuits of Figs. 2 and 3, it is difficult to make a comparison of a complex CM circuit with a VM circuit.

III. VM-CM PAIR

Many of the filters in the past used high-gain heavily-compensated operational amplifier (OA) as an active device with feedback to render the low sensitivities due to the non-idealities of the devices. These filters show a substantial degradation of performance at higher frequencies. Several filters {[1]-[12] of [1]} were proposed that did not use high-gain OAs. They operated at much higher frequencies than the OA-based filters. Many of these filters also inherently performed well with reduced power supply voltages. Later, some researchers used port currents rather than port voltages. A large number of analog circuits using VM devices such as OAs have already been developed with elegant designs. It is worth deriving the CM filters from VM filters.

We will call the VM-CM pair if one circuit is derived from the other such that the transfer functions V_o/V_i and I_o/I_i are identical. These operations will be expressed as $\tau(\text{VM}) = \text{CM}$, $\tau(\text{CM}) = \text{VM}$. Since the output-input relations are the same for VM-CM pair, the responses of the two circuits bound to be the same.

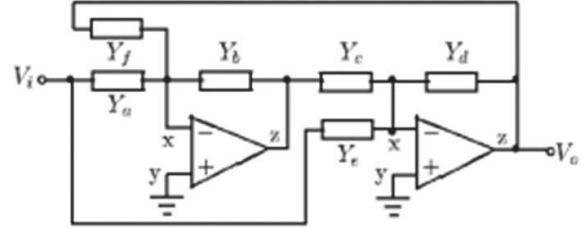


Figure 4. Lovering VM circuit.

We will review various methods proposed for obtaining VM-CM pair. In some of the methods, we will use Lovering VM circuit [3] shown in Fig. 4. The transfer function of the circuit is

$$\frac{V_o}{V_i} = \frac{Y_a Y_c - Y_b Y_e}{Y_b Y_d - Y_c Y_f} \quad (1)$$

Robert and Sedra VM-CM Pair: Robert and Sedra [4] proposed the VM-CM pair using adjoint network concept. A network is considered reciprocal when the same input-output transfer function results if the excitation and the response are interchanged. Not all the networks possess this reciprocal behaviour. However, if the adjoint of a network N is N_a , then the circuits of Figs. 5(a) and (b) exhibit the same transfer function.

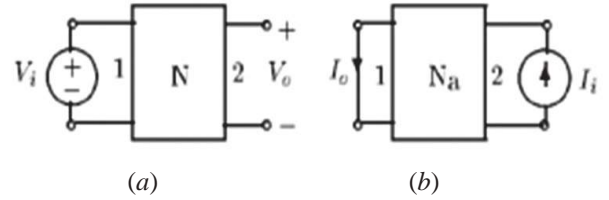


Figure 5. Two circuits that have $V_o/V_i = I_o/I_i$

Robert *et al.* [4] have presented inter-reciprocal pairs of some basic active building blocks shown in Fig. 6.

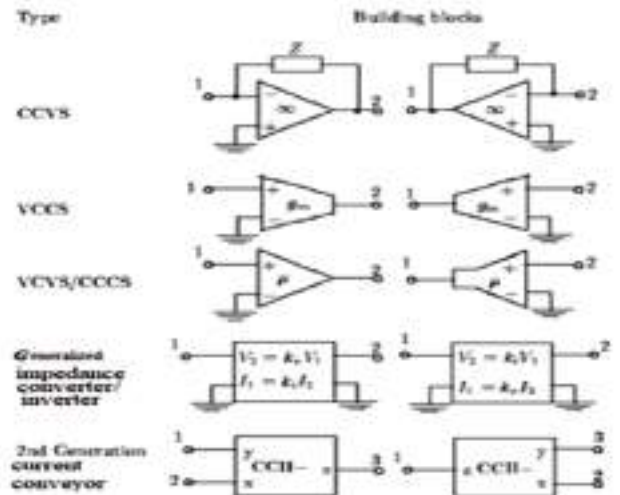


Figure 6. Inter-reciprocal active circuit building blocks using adjoint blocks.

The procedure for $\tau(VM)$ operation is: Replace each block of the VM circuit by its corresponding adjoint block. Input voltage source at port 1 is replaced by a output short circuit current I_o . A current source I_i is connected to port 2. Hereafter, last two steps together will be referred as input-output source replacement (IOSR) operation. Following the above steps, the CM circuit of Lovering VM Circuit is shown in Fig. 7.

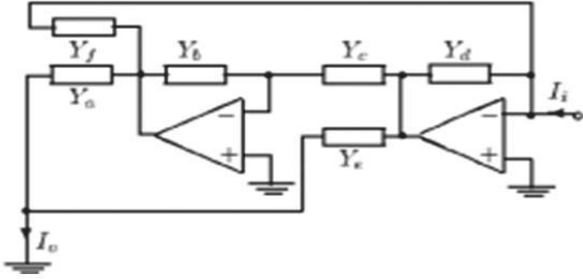


Figure 7. Robert and Sedra CM circuit of VM circuit of Fig. 4.

Uzunhisarcikli and Alci $\tau(VM)$ Operation: Uzunhisarcikli and Alci [8] suggested procedures for obtaining CC- and FTFN CM circuits from OA circuits. CC version: (i) Replace the OA together with the feedback element by its CC equivalent circuit. (ii) Replace each CC by its nullor equivalent. (iii) Interchange the nullators and norators of each CC. (iv) Perform IOSR. (v) Replace nullators and norators back to CCs to get the CM circuit.

FTFN version: Replace each of the OAs directly to nullor equivalents and follow the above steps (ii)-(iv). Replace nullators and norators by their FTFN structure. The CM circuits corresponding to the Lovering VM circuit are shown in Fig. 8(a) and (b). Uzunhisarcikli and Alci and

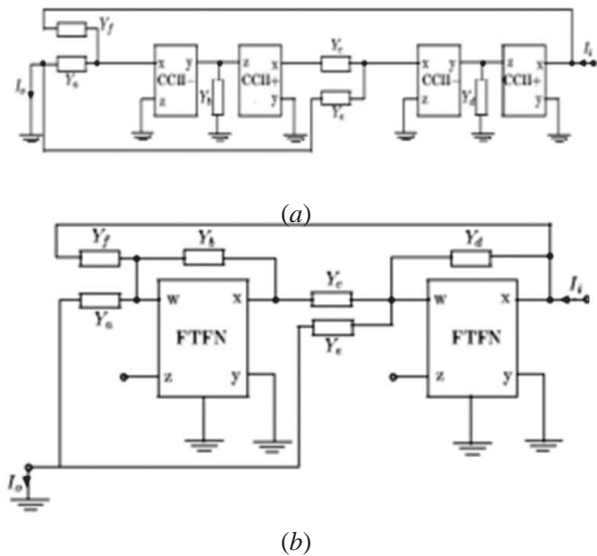


Figure 8. Uzunhisarcikli Alci CM circuits using (a) CC, (b) FTFN

Carlosena and Moschytz VM-CM pair: Carlosena and Moschytz [6] proposed $\tau(VM)$ operation as follows. Replace each controlled source by its nullator-norator equivalent. Interchange nullator and norator of each controlled source. Perform IOSR. Finally, replace each nullator-norator pair by a corresponding OA. Following the above steps, the CM circuit of Lovering VM.

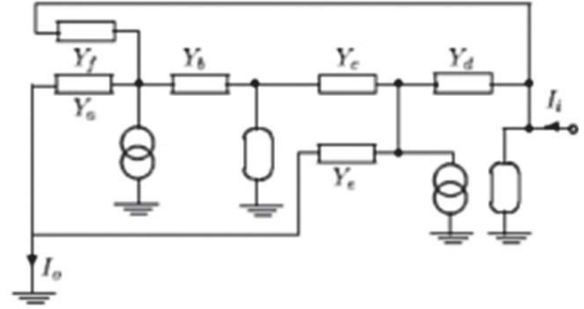


Figure 9. Carlosena and Moschytz CM circuit of the Lovering VM Circuit.

Circuit is shown in Fig. 8. All the above three methods involve use of nullator-norator pairs.

Aronhime and Lata $\tau(VM)$ Operation: Aronhime and Lata [7] suggested the procedure from an OA VM to an OA CM circuit. Remove all the input impedances by short circuits. Apply input current source I_i . Connect admittances from the output of each OA to a common point. The current flowing from this common point to ground is the output current I_o . Find the transfer function I_o/I_i . Determine the conditions so that $I_o/I_i = V_o/V_i$. From these, find the values of the admittances added. Thus, the Lovering CM circuit obtained is shown in Fig. 10. The transfer function of the new circuit is

$$\frac{I_o}{I_i} = \frac{Y_c Y_h - Y_d Y_g}{Y_b Y_d - Y_c Y_f} \quad (2)$$

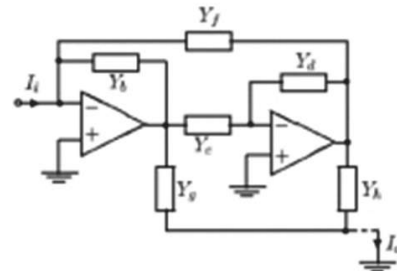


Figure 10. Aronhime Lata CM circuit.

This is not the same as the voltage transfer function given by (1). One possibility that the two become equal is when $Y_g = Y_b Y_e / Y_d$, $Y_h = Y_a$, provided Y_g is realizable as a driving

point admittance. Thus, the topology of the CM circuit is not the same as that of the VM one and requires additional elements which may not be realizable.

Rathore and Khot $\tau(\mathbf{VM})$ Operation: Consider the two circuits shown in Fig. 11 where N_a is the active network. Analysis of the circuits leads to the following relations.

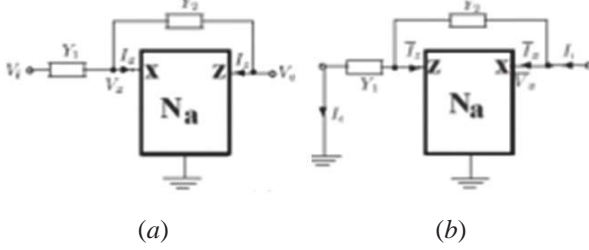


Figure 11.(a) VM circuit and (b) CM circuit.

$$\frac{V_o}{V_i} = -\frac{Y_1}{Y_2} + \frac{V_x}{V_i} \left(1 + \frac{Y_1}{Y_2}\right) + \frac{I_x}{V_i Y_2}, \quad (3)$$

$$\frac{I_o}{I_i} = -\frac{Y_1}{Y_2} + \frac{\bar{V}_x Y_1}{I_i} + \frac{\bar{I}_x Y_1}{I_i Y_2}. \quad (4)$$

Note that (3) and (4) are independent of I_z and \bar{I}_z , respectively. Thus, it is immaterial, whether there is a flow of I_z [\bar{I}_z] in the z terminal of the active device or not. For VM-CM pair, the condition is, from (3) and (4),

$$\frac{V_x}{V_i} \left(1 + \frac{Y_1}{Y_2}\right) + \frac{I_x}{V_i Y_2} = \frac{\bar{V}_x Y_1}{I_i} + \frac{\bar{I}_x Y_1}{I_i Y_2} \quad (5)$$

This can be satisfied under the following 2 cases.

Case A: Let

$$V_x = \bar{V}_x = 0, \quad I_x = \bar{I}_x = 0. \quad (6)$$

These terminal characteristics are satisfied when the active network N_a is an OA ($V_x = V_y$, $I_x = I_y = 0$), an FTFN ($V_x = V_y$, $I_z = I_x = 0$, $I_z = \pm I_w$) or a CCII \pm ($V_x = V_y$, $I_y = 0$, $I_z = \pm I_x$) shown Figs. 12, 13 and 14, respectively. Terminal x (y) is maintained at virtual ground by making V_y (V_x) = 0. For these circuits

$$\frac{V_o}{V_i} = \frac{I_o}{I_i} = -\frac{Y_1}{Y_2}. \quad (7)$$

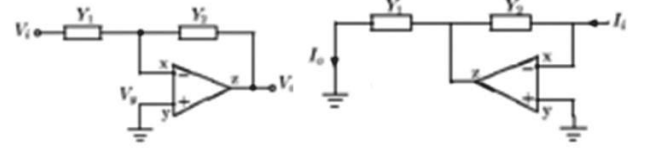


Figure 12. OA based VM-CM pair.

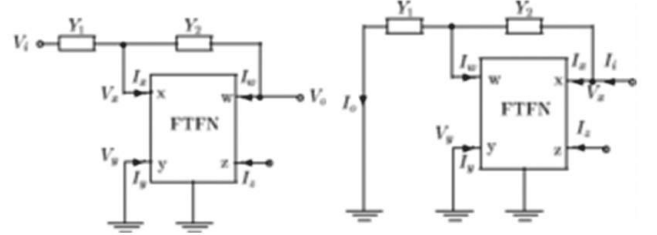


Figure 13. FTFN based VM CM pair

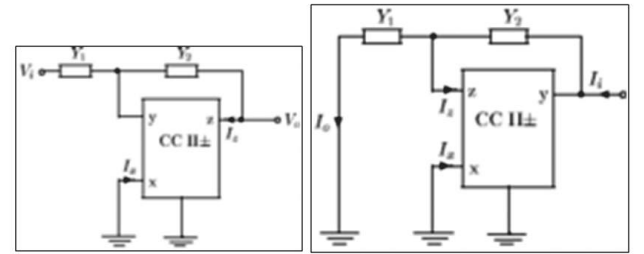


Figure 14. CC based VM-CM pair.

From these figures, it is clear that $\tau(\mathbf{VM})$ is executed by interchanging the terminals x and z in case of OA, the terminals x and w in case of FTFN, the terminals y and z in case of CCII, and then RIOS. Connections of passive elements remain unchanged.

Consider a multi-input (V_1 and V_2) VM circuit shown in Fig. 15(a) and its CM multi-output (I_{o1} and I_{o2}) circuit shown in Fig. 15(b). The output of the VM circuit is

$$V_o = \frac{Y_1}{Y_2} V_1 - \frac{Y_3}{Y_2} V_2. \quad (8)$$

Sub-networks A and B in Fig. 15(a) can be identified as the OA based multi-input blocks. The two current outputs of the CM circuit are

$$I_{o1} = -\frac{Y_1}{Y_2} I_i, \quad I_{o2} = -\frac{Y_3}{Y_2} I_i. \quad (9)$$

Sub-networks A and B in Fig. 15(a) can be identified as the OA based multi-input blocks.

Equation (9) is used for each building block in Fig. 15(a) and then solve for V_o/V_i . A corresponding circuit using the multi-output CM blocks is shown in Fig. 15(b). Equation (8) is used for each building block in Fig. 15(b) and solve for I_o/I_i .

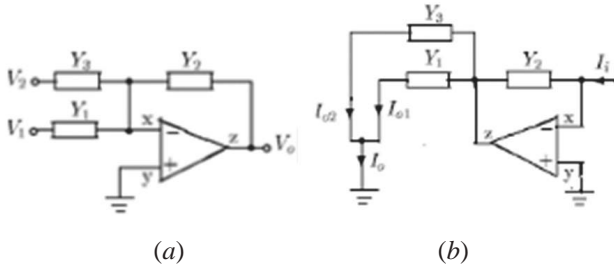


Figure 15. OA based (a) multi-input VM circuit and (b) multi-output CM circuit

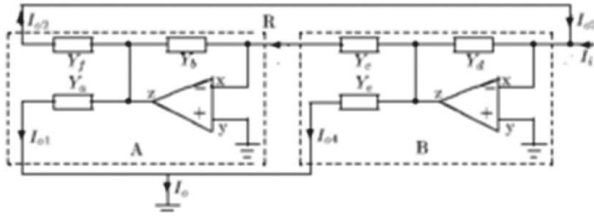


Figure 16. Covering CM circuit.

The procedure can be extended for $\tau(VM)$ operation to n OAs (each with the non-inverting terminal grounded) into OA-based CM circuits by interchanging x and z terminals of each OA, and IOSR operation.

Thomas biquad [10] VM-CM pair is shown in Fig. 17.

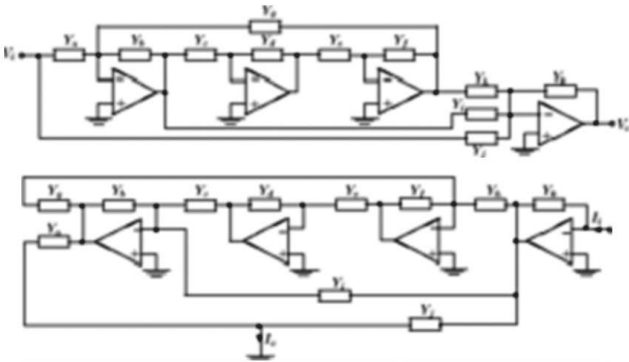


Figure 17. Thomas biquad VM-CM pair.

Case B: Let

$$V_x = \overline{V_x} = 0. \quad (10)$$

Under these condition, (5) reduces to

$$\frac{I_x}{I_x} = \frac{V_i Y_1}{I_i}. \quad (11)$$

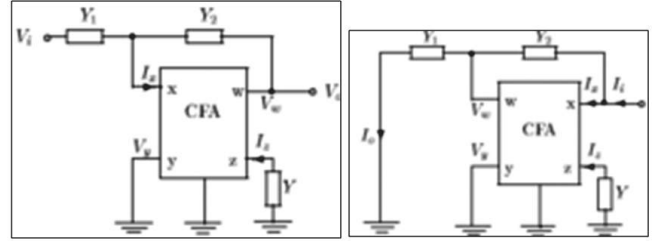


Figure 18. CFA based VM-CM pair.

Using the condition (7), we get

$$\frac{I_x}{I_x} = \frac{V_o Y_1}{I_o} = \frac{V_z}{V_x}. \quad (12)$$

This condition, and that in (10) are satisfied when the active network Na is a CFA ($I_z = I_x$, $V_w = V_z$, $V_x = V_y$) shown in Fig. 18. For both the Figs. 18(a) and (b), we have

$$I_x = I_z = -V_w Y = -V_z Y. \quad (13)$$

Thus, the current I_x , as desired for the operation $\tau(VM)$ to hold, satisfies the condition in (12). Now, from (3)

$$T(s) = -\frac{Y_1}{Y_2} + \frac{I_x}{V_i Y_2} = -\frac{Y_1}{Y_2} - \frac{V_w Y}{V_i Y_2} = -\frac{Y_1}{Y_2} - \frac{V_o Y}{V_i Y_2}$$

which leads to

$$T(s) = -\frac{Y_1}{Y_2 + Y}. \quad (14)$$

From Fig. 18 note that the CFA-based VM circuit (with terminal y grounded and the output tapped from the terminal w) can be converted into CFA-based CM circuit by interchanging the terminals x and w of the CFA, and IOSR operation. Connections of passive elements remain unchanged. Thus, the procedure is the same as that for the OA-based circuits under case A.

In a manner similar to the one used in case of OA-based circuits, it can be shown that the procedure is applicable to CFA-based VM circuits having a greater number of CFAs with terminal y grounded.

A VM-CM pair with a greater number of CFAs is shown in Fig. 19.

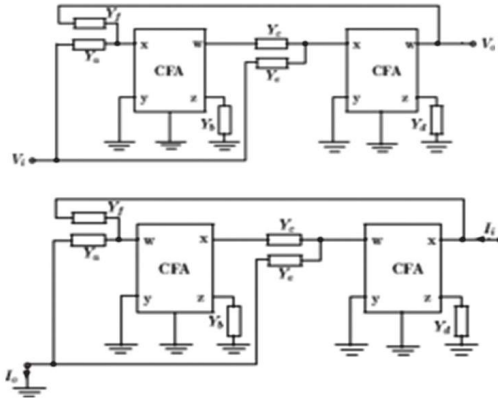


Figure 19. VM-CM pair with a greater number of CFAs.

IV. APPLICATIONS OF $\tau(VM)$ TO COMPLEX CIRCUITS

VM-CM pair of more complex circuits corresponding to the cases A and B are obtained from Figs. 12, by replacing 2-terminal passive elements by 3-terminal passive circuits NA and NB or N_B . This VM-CM pair is shown in Fig. 20. Analysis of these two circuits give

$$\frac{V_o}{V_i} = -\frac{Y_{21A}}{Y_{21B}} \quad (15)$$

and

$$\frac{I_o}{I_i} = -\frac{-Y_{21A}}{(-Y_{21B}) + Y} = -\frac{Y_{21A}}{-Y_{21B}} \quad (16)$$

Here Y_{21A} , Y_{21B} , and Y_{21B} are the transfer admittances of networks NA, NB, and N_B , respectively, and $Y_{21B} = Y_{21B} - Y$.

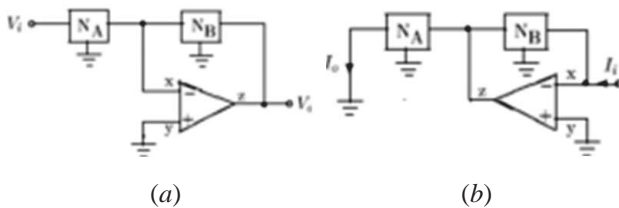


Figure 20. Generalized OA-based circuits (a) VM (b) CM.

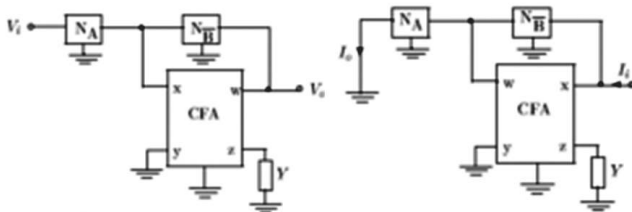


Figure 21. Generalized CFA-based VM-CM pair.

A close examination of (15) and (16) reveals that the following procedure can be used for converting OA-based VM-CM pair of Fig. 20 into CFA-based pair shown in Fig. 21 without

increasing the number of passive components. Take out a suitable driving point admittance Y from Y_{21B} of the OA-based circuit and realize the remaining admittance Y_{21B} as transfer admittance by the network N_B .

The OA-based VM low-pass filter shown in Fig. 22(a) is converted into four CFA-based CM low-pass filters shown in Fig. 22(b).

A VM-CM pair for the low pass filter with equal-valued grounded capacitors [11] is shown in Fig. 23.

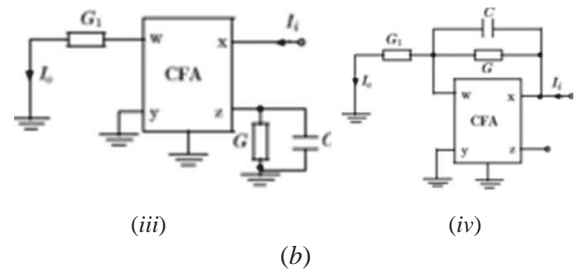
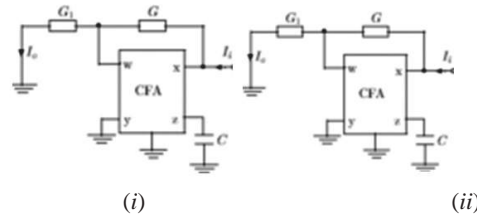
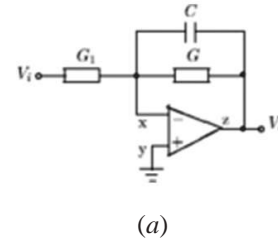


Figure 22. Low-pass filters (a) OA-based VM circuit; (b) four CFA-based CM circuits.

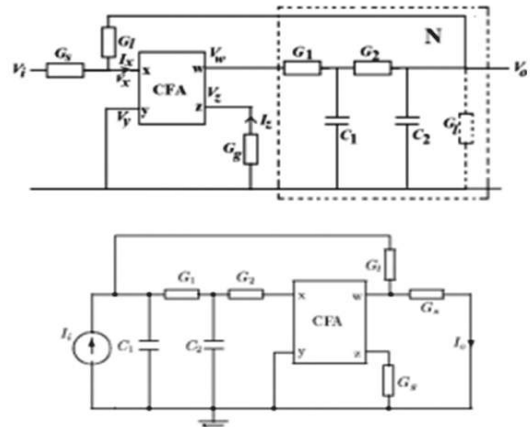


Figure 23. VM-CM pair of low-pass filter configuration.

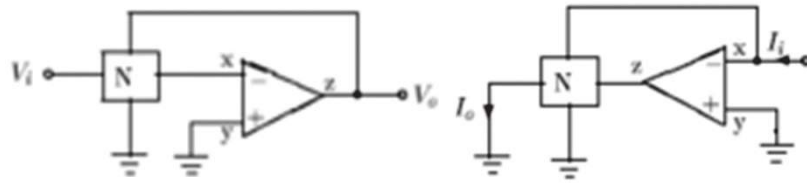


Figure 24. OA-based VM-CM pair with a 4-terminal passive network

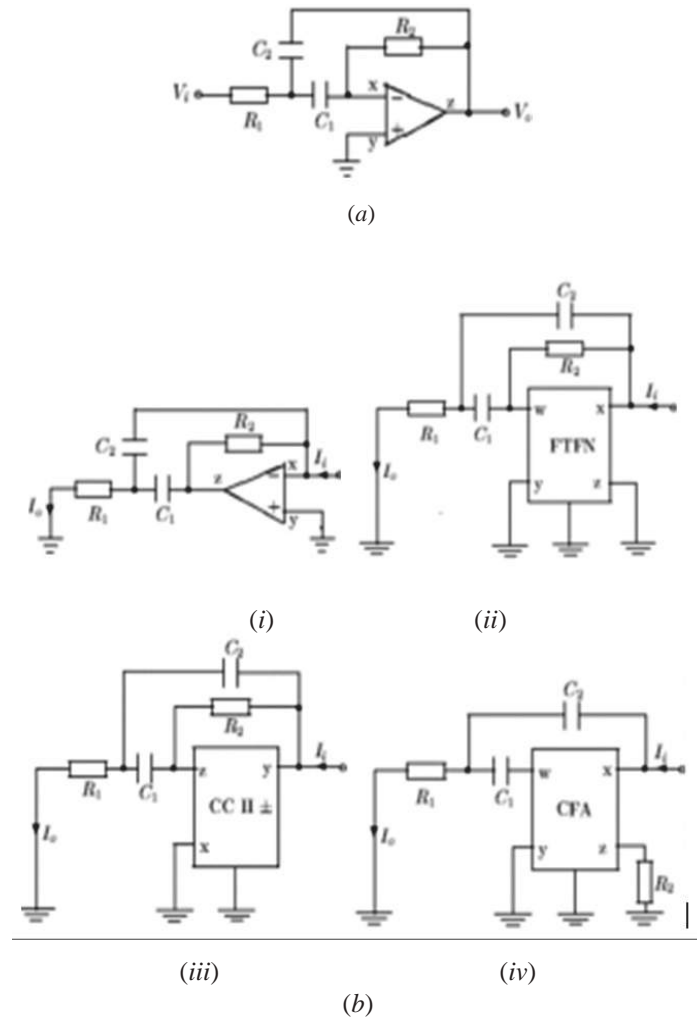


Figure 25. (a) OA-based VM band pass filter, (b) four CM band pass filters

The procedure outlined is also applicable to more generalized OA-based VM circuits shown in Fig. 24. $\tau(VM)$ operation on the VM band pass filter shown in Fig. 25(a) is converted in to four CM circuits shown in Fig. 25(b).

Rathore and Khot $\tau(VM)$ operation does not involve nullator norator pairs, require no additional elements. It maintains the same topology, and can handle various types of active devices. Also, it gives multi-CM circuits.

V. CONCLUSION

Advantage of CM circuits are mentioned. Various methods of obtaining CM circuits from known VM circuits are reviewed. Rathore and Khot $\tau(VM)$ operation does not involve nullator-norator pairs and require no additional elements. It maintains the same topology, and can handle various types of active devices. Theoretically, the performances of VM and CM circuits should be identical, however, a better high-frequency performance is obtained from CM circuits when physical

models of the active devices are considered. Because of the space constraint, we have not included the design of filters in direct CM domain. Interested readers may refer to [12]-[14].

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Dr. Tejmal Rathore received BSc (Engg), ME, and PhD (Electrical Engineering) all from Indore University, Indore. He served Shri Govindram Seksaria Institute of Technology and Science, Indore (1965-1978), Indian Institute of Technology Bombay (1978-2006), and St Francis Institute of Technology, Borivali (2006-2014) as Dean (R&D), and IIT Goa (2017-2019) as a Visiting Professor.

He was a post-doctoral fellow (1983-85) at the Concordia University, Canada and a visiting researcher at the University of South Australia, Adelaide (March-June 1993). He was an ISTE visiting professor (2005-2007). Published and presented over 225 research papers. Authored the book, *Digital Measurement Techniques*, Narosa Publishing House, New Delhi. 1996 and Alpha Science International Pvt. Ltd. UK, 2003 and translated in Russian language in 2004. He is the contributing author of the revised 3rd edition of the book *Network Analysis* by M E Van Valkenburg published by Pearson India Education Services Pvt. Ltd., Noida. He was the Guest Editor of the special issue of *Journal of IE on Instrumentation Electronics* (1992). He is a member on the editorial boards of *ISTE National Journal of Technical Education* and *IETE Journal of Education*. Prof. Rathore is a Life Senior Member of IEEE (USA), Fellow IETE and IE(I). Member of Computer Society of India and Instrument Society of India.